

Questa RDC – Reset Domain Crossing Verification

Automated solutions that target RDC verification challenges

Benefits

- Easy Set Up
 - Direct reuse of Questa CDC RTL-level setups, constraints, waivers, and results
 - Built-in support for SDC files, Liberty models, and UPF specifications
- Easy to Use for Both Novices and Experts
 - Automatically infers clock and reset signal groupings
 - Automatically identifies and regroups logic belonging to RDC and reset synchronization structures
 - Supports more than 20 synchronization styles
 - Creates custom synchronizers for proprietary synchronization styles

Features

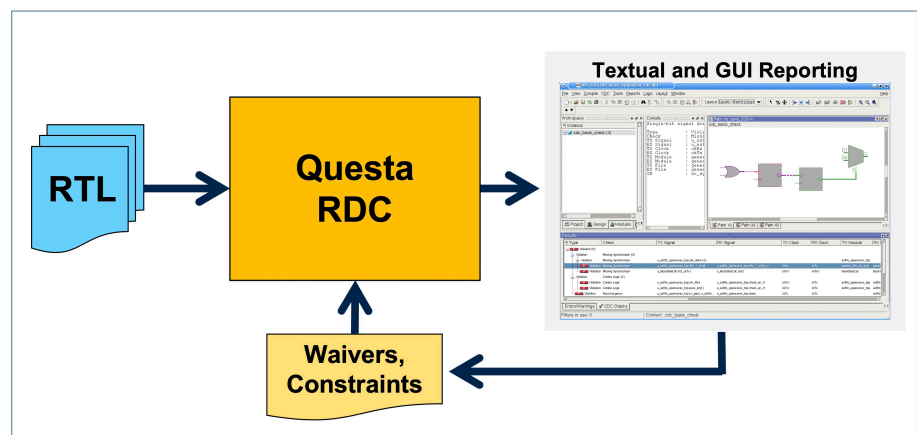
- Automated, Exhaustive Analysis
 - Runs deep formal analysis on automatically generated assertions
 - Integrates structural, functional, and formal algorithms to verify RDC structures

Reset Domain Crossings Require Sophisticated, Exhaustive Analysis

Designers increasingly use complex reset signaling architectures to meet high-performance, low-latency, and low-power requirements. The increase in reset signaling complexity, along with the emergence of multiple reset signaling networks in devices, is

creating new verification challenges that cannot be addressed by RTL simulation. Specifically, independent reset domains are created by complex reset sequences, reset circuitry, and the intermixing of IPs with different reset schemas, power-management domains, and security domains or functionality.

The asynchronous reset domain crossings (RDC) that arise create metastability and signal reconvergence issues in the reset signaling networks — similar to the failures seen in asynchronous clock domain crossings (CDC). Just as with CDC phenomena, the metastability induced by these asynchronous RDCs cannot be modeled or exhaustively covered by digital simulation, leaving designers open to the considerable risk of unpredictable chip behavior when samples come back from the fab, or worse, when in the field.



Using only your RTL as input, Questa RDC uses formal methods to statically and exhaustively identify reset domain crossing issues.

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Features *continued*

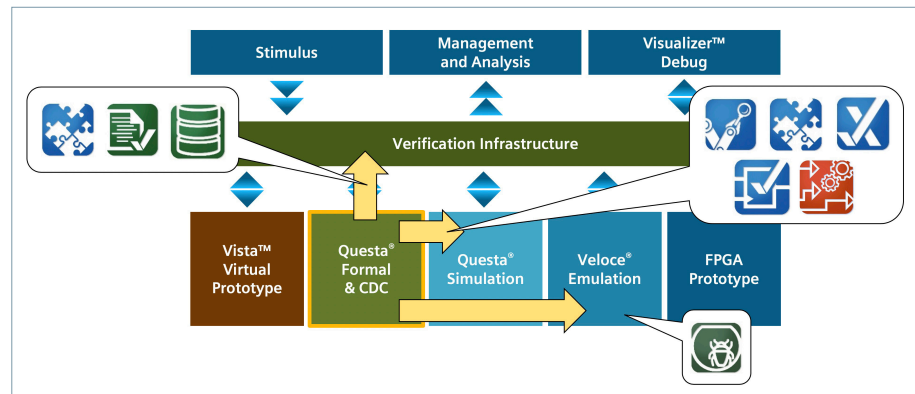
- Easy Result Analysis and Debug
 - Waiver management flow enables violation and waiver tracking throughout the design process
 - Powerful Tcl API for targeting RDC data for custom reports
 - Questa Verification Manager integration automatically generates test plans and trend reports
- Power Aware RDC Verification
 - Supports UPF 2.0 and 2.1
 - Considers all isolation and retention cells
 - Reconvergence verification

Automated, Easy-to-Use RDC Verification

Questa® RDC identifies reset domains, the related clock domains, and reset domain synchronizers, as well as low power structures via the Unified Power Format (UPF). The technology then exhaustively checks for any potential RDC errors, statically verifying that all signals crossing asynchronous reset and clock domain boundaries are guarded by RDC synchronizers. Any discovered issues are illustrated using familiar schematic and waveform displays.

Industry-Leading Scalability and Quality of Results

When analyzing billion gate designs, minimizing noise is critical — i.e., how many issues does RDC analysis report and are these issues real or false positives. Questa RDC builds upon the CDC path and waiver information from Questa CDC analysis, then executes a comprehensive, formal-based analysis that works through all design elements for high throughput and noise minimization. This simultaneously provides industry-leading scalability and high quality of actionable results, while enabling RDC IP reuse.



The Enterprise Verification Platform

Benefits and Highlights

Rapid Bring-Up — Direct reuse of Questa CDC RTL-level setups, constraints, waivers, and results enables reset domain and clock groupings to be automatically inferred and reported. Automated incorporation of synthesis design constraints (SDC), Liberty models, and Unified Power Format (UPF) specifications further expedites bring-up.

Ease of Use — Reset signaling and clock groupings are automatically inferred and reported with each run to confirm there are no unexpected changes. Questa RDC pinpoints all potential RDC issues and automatically identifies any existing RDC synchronization structures. No test-bench is required.

RDC Repair Guidance — Questa RDC offers over twenty synchronization styles. Custom synchronizers can be created for proprietary synchronization strategies.

High Accuracy, Fast Results — Questa RDC produces the fewest RDC false negatives in the industry to prevent wasted time chasing non-issues.

Familiar Visualization — RDC-centric analysis and debugging GUI leverages familiar schematics and waveforms.

SoC-Level Scalability — Questa RDC high-performance analysis can process billion-gate designs.

High Performance Analysis — Questa RDC exceeds customer expectations in scalability, performance, and resources due to continuous investments in research and development.

The Enterprise Verification Platform

Built upon several powerful technologies and tightly integrated with Veloce® emulation, the Enterprise Verification Platform transforms verification, dramatically increasing productivity and more efficiently managing resources. The Questa CDC and Formal solutions are integrated with simulation and emulation, sharing common features such as verification management, compilers, debuggers, and language support for SystemVerilog, Verilog, VHDL, UPF, and more. This enables users to select the best application or tool for the job, and then combine results from all the engines to dynamically track the progress of the entire verification program.

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