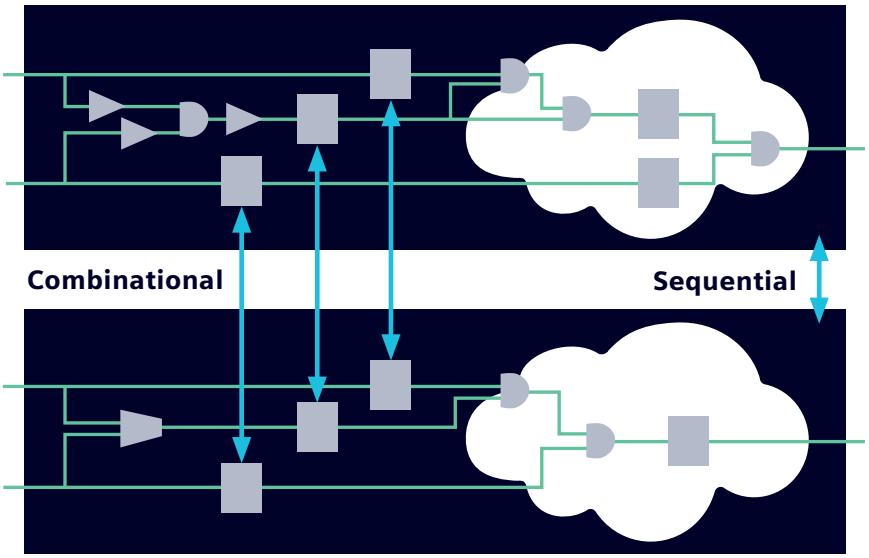
DIGITAL INDUSTRIES SOFTWARE

Questa Equivalent FPGA

FPGA optimized sequential equivalence checking

Formal verification of highly optimized FPGAs

The Siemens Questa™ Equivalent FPGA solution ensures that FPGA implementation flows, such as synthesis and place-and-route optimizations, do not introduce functional errors. The sequential equivalence checking technology provides key advantages over basic combinational equivalence checking and enables the user to achieve competitive improvements in functionality, performance, power consumption and cost targets through the incorporation of advanced implementation flow optimizations with full confidence in the resulting function. Further, verification time and cost savings are realized through the minimization of gate-level simulation and rapid identification of latent and difficult to detect design flow bugs. Questa Equivalent FPGA is used extensively by FPGA teams focused on A&D, automotive, high-reliability and safety critical applications.



Questa Equivalent FPGA provides the combined power of sequential and combinational proofs for FPGAs.

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Verification flow

Questa Equivalent FPGA follows a multi-step verification flow consisting of design set up, mapping and comparison and debug (optional).

The underlying sequential equivalence checking technology provides FPGA optimized equivalence checking capabilities that are unique in the industry:

- **Set up:** automated load settings and verification scripts simplify the configuration of the flow for respective FPGA vendors, devices and synthesis tools
- **Mapping:** comprehensive pairings of RTL to gate-level registers are not required to provide conclusive results
- **Comparison:** multiple sequential verification engines are leveraged to rapidly prove equivalence or generate counterexamples, independent of mapping of other comparison points
- **Debug:** failing simulation patterns generated on demand to rapidly identify hard to detect functional bugs

Advanced FPGA synthesis optimizations are supported including:

- Stuck-at (constant) registers
- Fixed gated clocks
- Register duplication and merging
- DSP optimizations
- FSMs with safe and unknown encodings
- SRL optimizations, including reset registers
- RAM/ROM inference and register packing, including distributed and block RAM
- Asynchronous feedback loops
- Power optimizations
- IO cells and different bus resolution schemes
- Pipelining

Questa Equivalent FPGA feature overview

FPGA vendor support

- AMD-Xilinx
- Intel
- Microchip

Design language

- Mixed language support, Verilog/SV/VHDL

Supported platforms

- Linux 64 Bit
- RHEL
- SUSE Linux Enterprise Server
- CentOS
- Windows 64 bit

General

- Dedicated mapping management window with scratch pad and separate tabs for inputs, outputs and internal signals
- Highly automated proof strategies
- Compare results/update mapping management window
- Constraints management window
- Separate counterexamples tab
- Value annotation of code by selecting specific counterexamples

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85575-D2 12/23 C