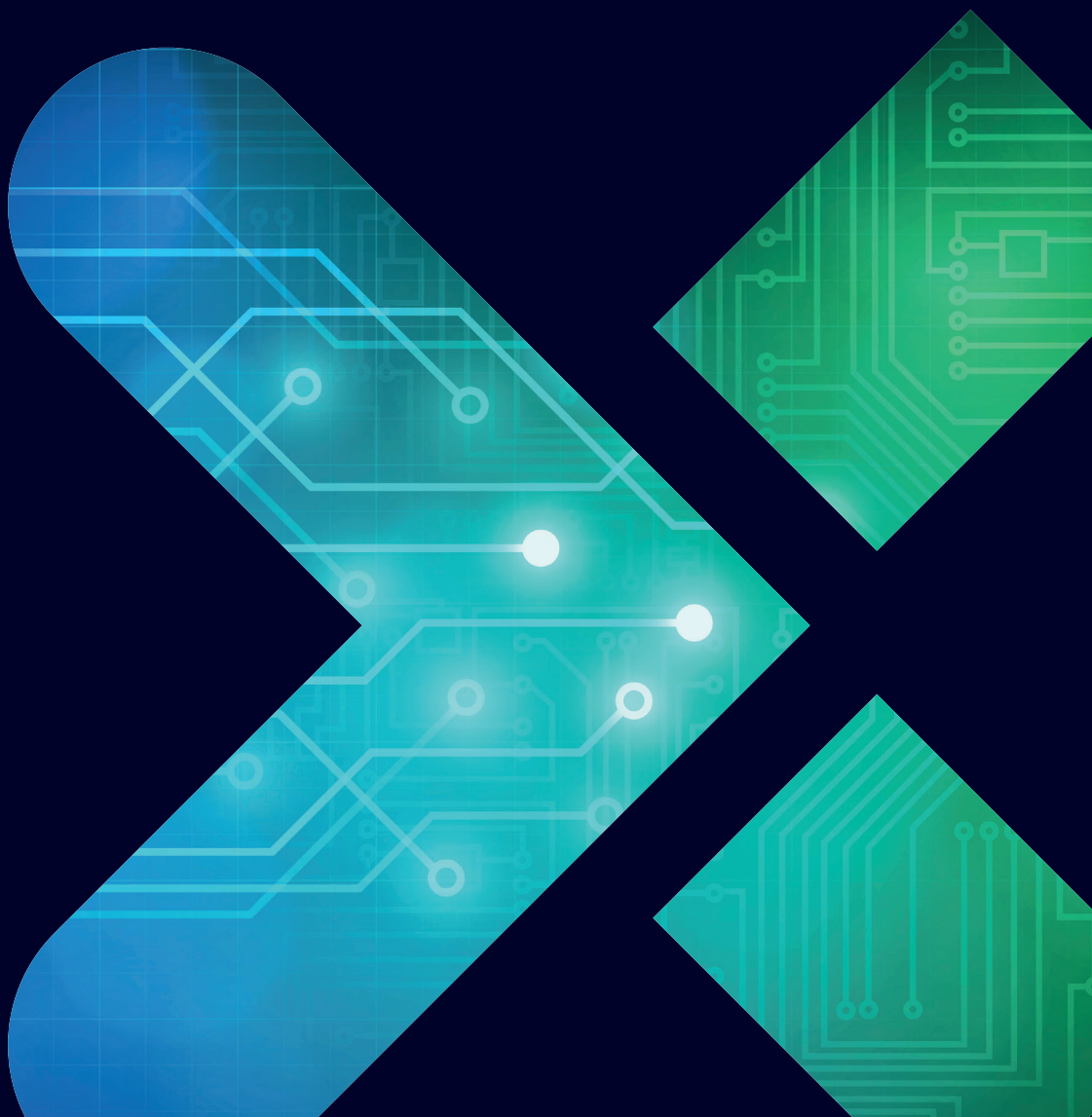
SIEMENS

DIGITAL INDUSTRIES SOFTWARE

HyperLynx

Equipping enterprise engineering teams to handle complexities in electronics systems design

siemens.com/pcb



Announcing next-generation electronic systems design

The next generation of HyperLynx introduces an industry-leading intuitive modern user experience, creating an adaptive and agile environment that enhances user productivity and accelerates the design process.

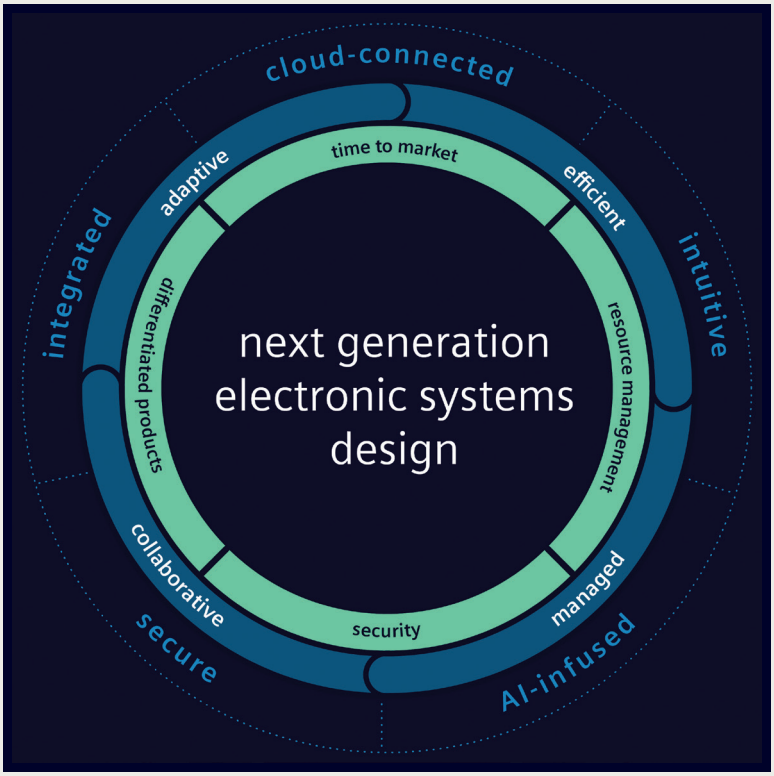
Intuitive
The full HyperLynx portfolio offers the latest modern-UX principles, which include personalized user interfaces and command search engines.

AI-infused
Artificial intelligence-enabled design boosts productivity, bridging capacity gaps within development teams and enabling them to tackle complex challenges effectively.

Cloud connected
Facilitating collaboration across the entire ecosystem, from component selection to manufacturing, the next generation of electronic systems design offers a cloud connected environment to ensure seamless communication and coordination.

Integrated
HyperLynx supports the digital transformation of electronics system design by integrating digital threads across multiple domains, providing a comprehensive view of the entire design process.

Secure
Recognizing the importance of compliance with commerce and government regulations, the next generation of electronic systems design offers managed access within a secure environment, ensuring the protection of sensitive information.



High-speed analysis tools for high-speed designs

HyperLynx equips you to succeed today and tomorrow.

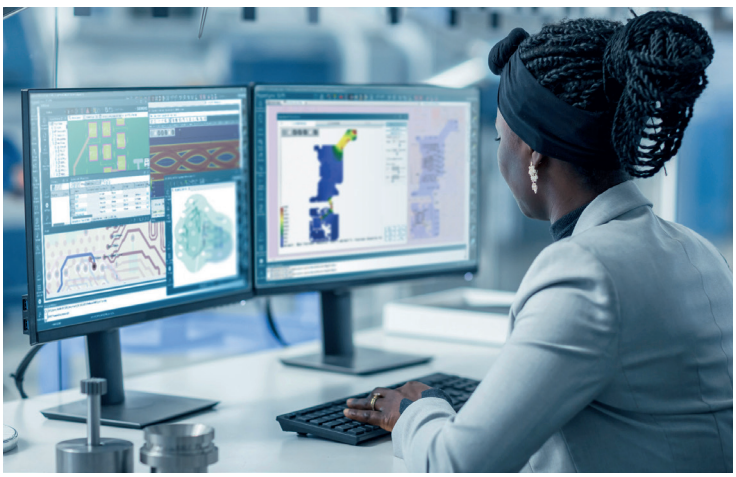
According to the January 2025 Electronic Design Market Data (EDMD) report by the ESD Alliance, a SEMI Technology Community, printed circuit board and multichip module design software revenue rose 5.8% year-over-year to $450.8 million in the third quarter of 2024. This boosted the four-quarter moving average (which compares the most recent four quarters to the prior four) for PCB and MCM up to 9.1%.[1] As the PCB market and PCB complexity continue to grow, the need for signal and power integrity analysis has become pervasive. Anticipating this trend, HyperLynx delivers a complete, integrated family of analysis tools that cover the entire electronic systems design process – from schematic capture and exploration through post-layout verification.

Equipped with proven automated analysis workflows and examples, HyperLynx delivers productivity right "out of the box." Design simulation, verification analysis, and performance optimization ensure that the finished design is ready for the next step of the design process.

You gain the full power of HyperLynx when it is fully integrated as part of the Xpedition PCB design flow. Yet, it also interfaces with most PCB layout tools, allowing any engineer to quickly import and set up their PCB designs for analysis, regardless of their existing toolset. And because its progressive verification methodology analyzes a design in stages, HyperLynx locates issues earlier and faster, without involving SI and PI experts, no matter how simple or complex your design. So whatever layout tool you use and regardless of individual skill levels, HyperLynx makes design analysis and high-speed, post-layout verification easier for every user.

The earlier verification analysis is performed in the design process, the better, and HyperLynx doesn't make you wait. Sections of the design can be verified and implemented so that issues can be identified and resolved, even before the schematic or board layout is complete. Finding problems early means that other sections of the design aren't affected, as is often the case when analysis can only be performed once the design is complete.

There's no point in running SI/PI simulations if the tools you're using don't have the accuracy, capacity and performance to do the job in a reasonable timeframe. HyperLynx Power Integrity (HL-PI) uses the same interface as HyperLynx Signal Integrity (HL-SI), so it's easy to switch back and forth between signal and power integrity analysis.



1. Circuit Assembly, 1-14-2025, circuitsassembly.com/ca/editorial/menu-news/41591-pcb-design-software-sales-reach-450m-in-q3.html

Progressive verification with HyperLynx

Avoiding analytical overkill is critical to completing projects on time.

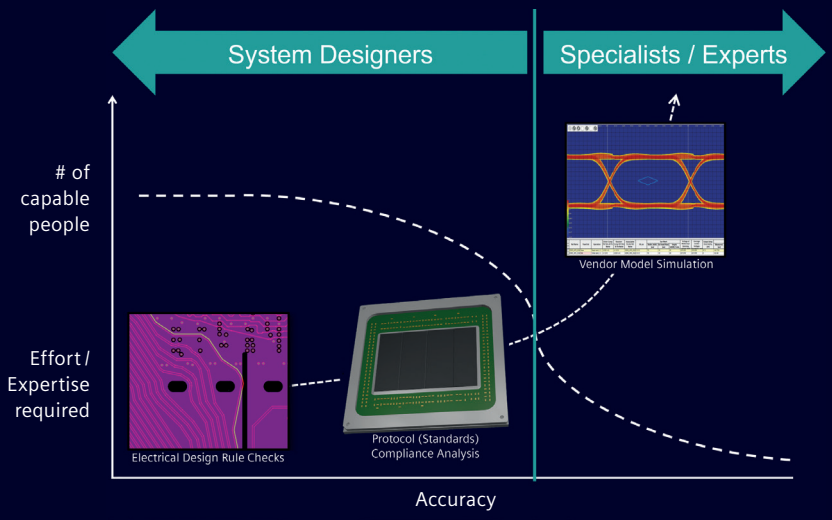
Companies typically rely on experts to run PCB design analysis, whether in-house or via a consulting firm. But that, in turn, creates a bottleneck at the analysis stage: you don't want your experts spending time on the easy stuff. Instead, to ensure efficient use of time and resources, you need to focus expert efforts on the most challenging problems.

Progressive verification is a dynamic and strategic approach to verification that allows design teams to efficiently manage their resources and reduce the risk of project delays. With progressive verification, tasks are divided into three categories: quick tasks, intermediate tasks, and complex tasks. Quick tasks involve automated rule-based verification, while intermediate tasks focus on compliance analysis using generic technology-based models. Both of these can be handled by design teams. Complex tasks require detailed modeling and vendor-specific component models and settings, so they are typically handled by signal integrity experts.

This approach not only helps in catching errors early but also alleviates the bottleneck created by having to rely on external or in-house experts. Enabling PCB designers to take control of the verification process ensures that issues are identified and resolved throughout the design cycle, and experts' time is only taken up by the most complex problems.

HyperLynx uses the progressive verification methodology, with built-in, fully automated analysis flows that make your job easier by ensuring that analysis is always performed consistently. It includes a unified pre/post layout workflow for ease of design and verification efficiency and is easy to use for people who don't perform signal and power integrity analysis for a living.

Ultimately, progressive verification enhances the ability of design teams to meet stringent deadlines without compromising on quality.



Progressive verification methodology.

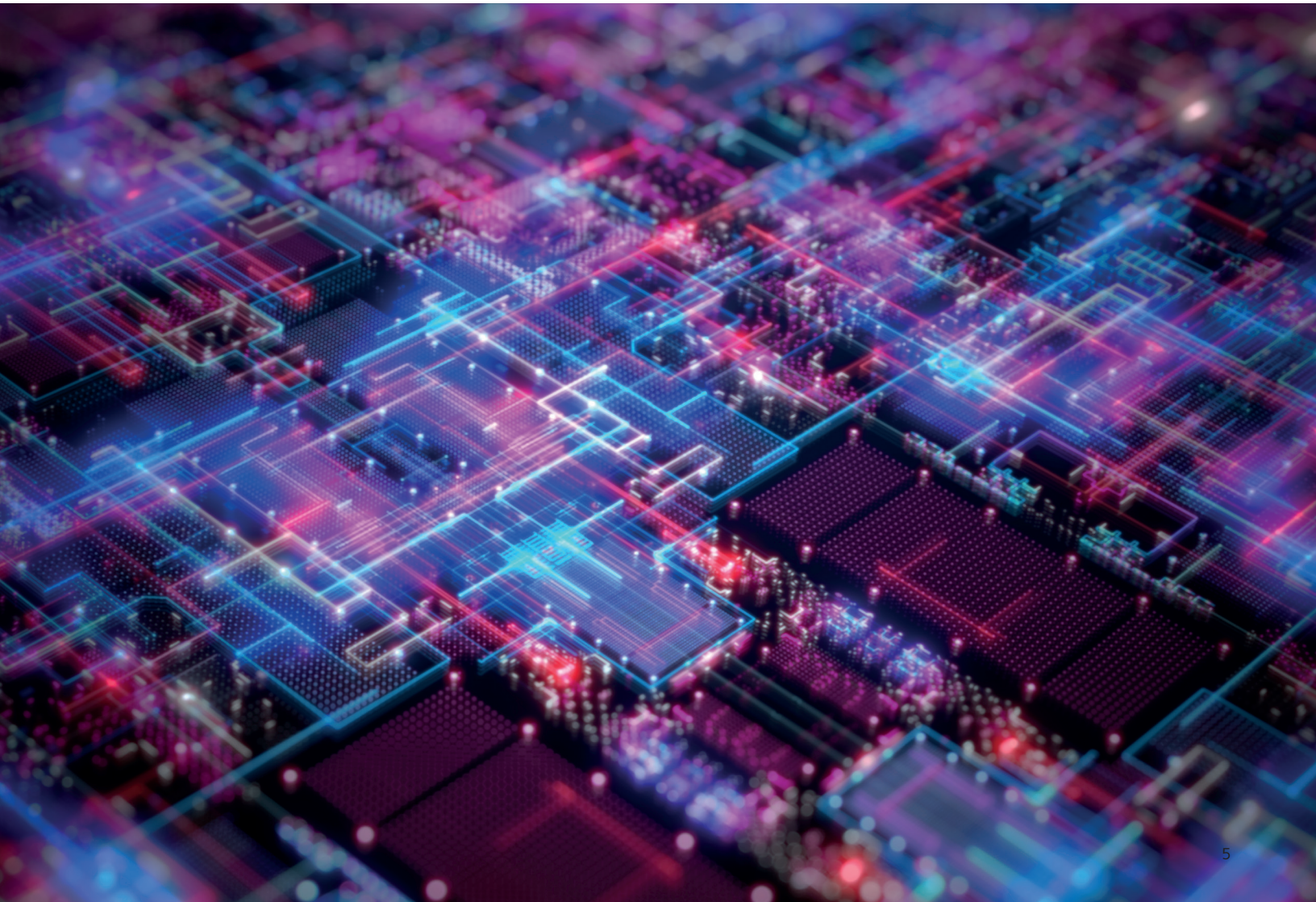
HyperLynx verification and analysis

Accelerate your analysis and verification applications.

HyperLynx supports progressive verification in several key applications:

- Rules-based verification
- Analog/mixed-signal analysis
- Power integrity analysis
- Signal integrity analysis
- Electromagnetic simulation
- Stackup design

For each of these applications, HyperLynx offers a set of tools that can be run standalone or together for a complete analysis and verification workflow.



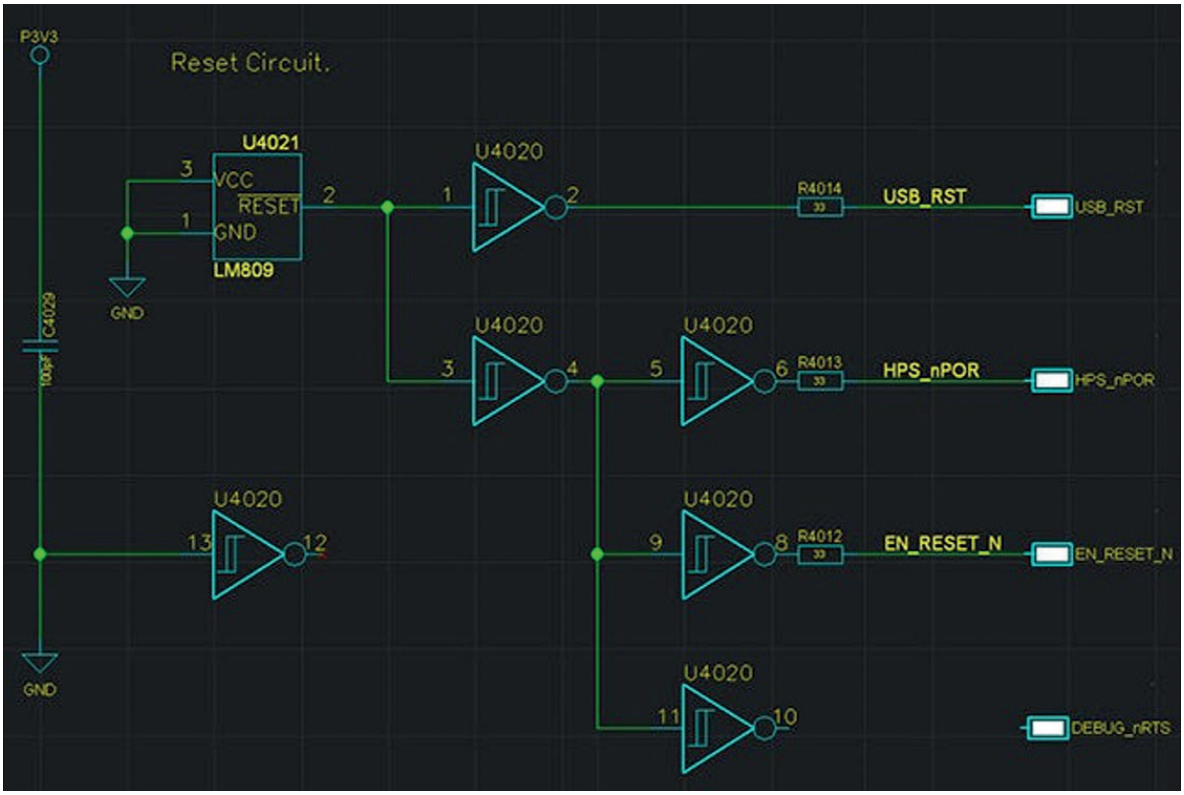
Rules-based verification

Rules-based verification replaces traditional manual design reviews with automated scanning of a design based on configurable rules, identifying possible design issues quickly and accurately. With the HyperLynx rules-based verification toolset, analysis is fast, results are targeted, and identification of problems occurs much earlier and easily than when using modeling and simulation.

HyperLynx Schematic Analysis (HL-SA)

HyperLynx Schematic Analysis provides fast and efficient schematic verification, allowing users to locate problems faster and easier without the need for in-depth simulation tools. All nets on a schematic are fully inspected using an extensive model library, eliminating hundreds of hours of manual inspection and lab debug time. HyperLynx Schematic Analysis allows you to organize and visualize schematic errors quickly and easily, while reducing design spins and improving product quality.

HyperLynx Schematic Analysis eliminates the need for manual schematic reviews and increases overall workflow efficiency by providing automated schematic reviews in parallel with design capture, with errors highlighted directly in the schematic. By adopting a "right first time" design flow, HyperLynx Schematic Analysis reduces development, testing and warranty costs, eliminating 50-70% of design respins caused by schematic errors and poor design practices. Schematic analysis can also be performed on electronic designs after they have been released into the market.

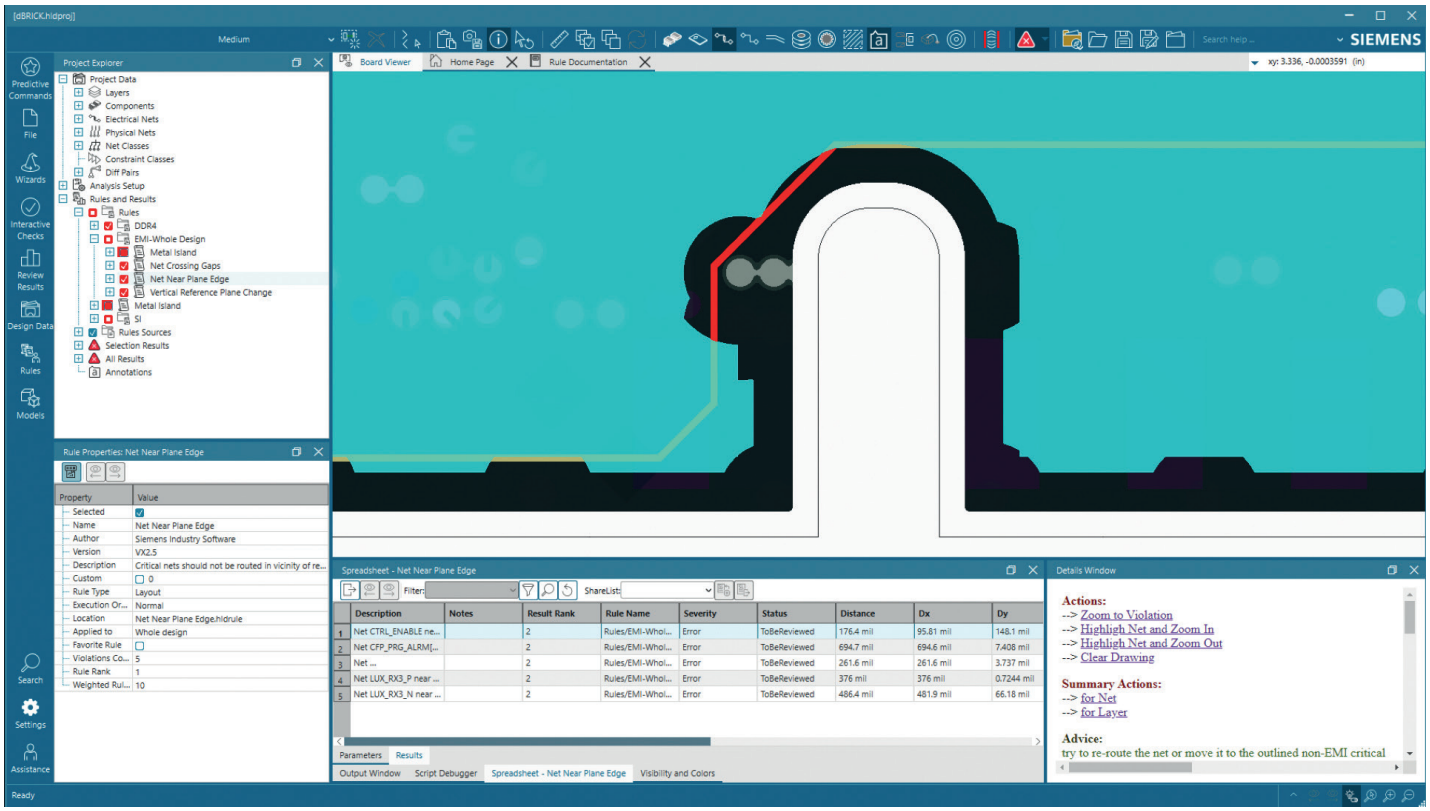


HyperLynx DRC (HL-DRC)

HyperLynx DRC quickly finds problems that are difficult, time-consuming and expensive to find through simulation, including signal traces crossing antipads and plane splits, signal return path issues and compliance with electrical safety requirements.

HyperLynx DRC replaces visual post-layout inspection with fast, automated design rule checking that quickly and accurately identifies potential problems related to analog, EMI, signal integrity, power integrity, packaging, and compliance-based electrical safety. HL-DRC creates a detailed list of items for interactive review, with the ability to zoom in on the layout view to display each issue and highlight problem areas graphically.

HyperLynx DRC's unique 3D geometry engine allows it to check complex physical and electrical design problems quickly, allowing those problems to be resolved without utilizing dedicated signal integrity experts. By quickly taking many potential problems "off the table," detailed modeling and simulation efforts will be time well spent.



Analog/mixed-signal analysis

HyperLynx provides a digital-twin environment for system design and analysis by enabling mixed-signal/mixed-domain analysis through support of SPICE and VHDL-AMS simulation models for time-domain simulation.

HyperLynx AMS

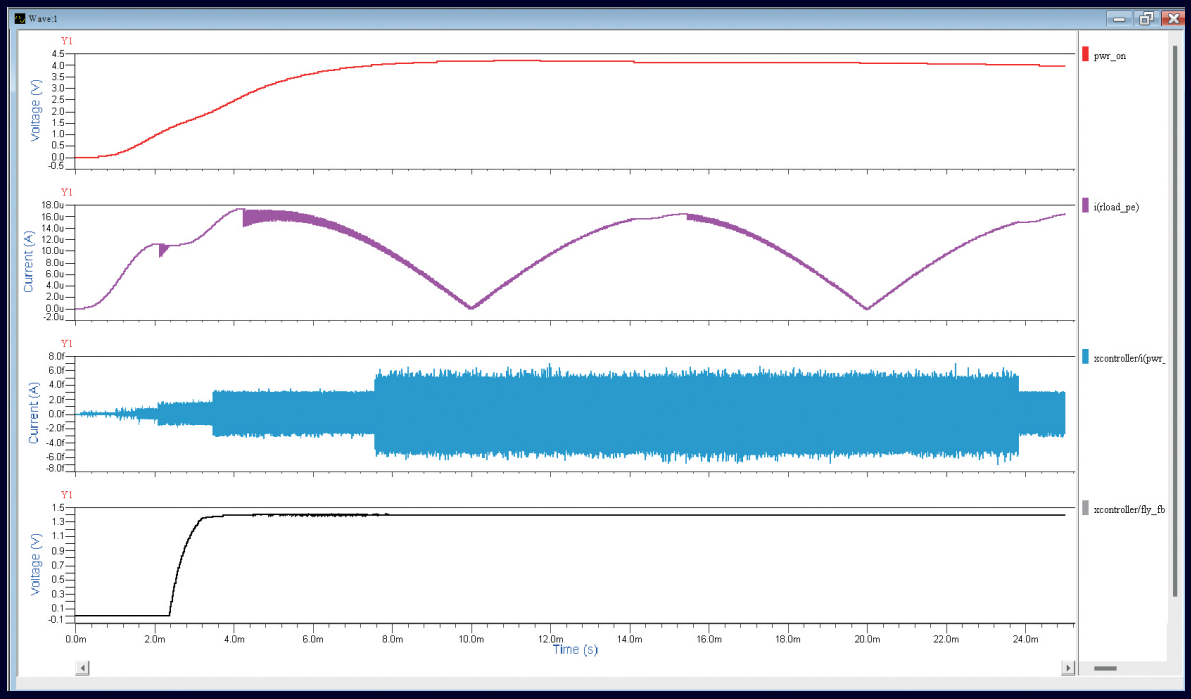
HyperLynx AMS expands standard SPICE-based circuit analysis to include modeling and simulation of electro-mechanical, thermal, and other domains in the broader system context. Driven from the same schematics used for PCB layout and capable of including the effects of PCB layout in simulations, HyperLynx AMS provides a virtual environment for circuit design and analysis that will accelerate your design and verification process.

HyperLynx AMS models electro-mechanical and other disciplines in a broader system context than is normally supported by time-domain circuit simulation. It supports advanced parametric analyses to verify design performance beyond nominal conditions and uses full-featured data measurements to quantify design performance metrics.

HyperLynx AMS is tightly integrated with the Xpedition design flow, so the same schematic used to drive simulation also moves your design seamlessly to layout.

Advanced design simulation allows you to extend standard time and frequency domain analysis to explore design sensitivities, sweep circuit parameters, determine manufacturing yields, and analyze worst-case performance. You can verify your design's performance using a virtual prototype of the target system, resolving issues and optimizing performance before committing it to fabrication.

Because it is integrated with PCB layout tools, HyperLynx AMS allows the effects of PCB layout topologies on analog and mixed-signal performance to be included in simulations, analyzing the board as it will be actually built.



Power integrity analysis

Higher layer counts, tighter margins, lower voltages, and increasing power consumption make power integrity analysis an essential component of modern system design.

HyperLynx PCB power integrity (PI) analyzes the behavior of a design's PCB at both DC and AC to ensure that components get the power they need, at the voltages they need, at the frequencies they need. Both DC and AC power integrity are supported from the same GUI, so a design can be set up once and analyzed for both DC and AC power delivery network (PDN) behavior.

HL-PI can import layout data from a wide variety of CAD formats for analysis. Once the database is imported, analysis wizards guide users through different analysis flows step-by-step, making sophisticated power integrity analysis directly available to mainstream designers who can perform simulations and make design decisions as part of their regular design cycle. The HyperLynx PI tool suite includes several powerful technologies that make proper power delivery an easier, more efficient task.

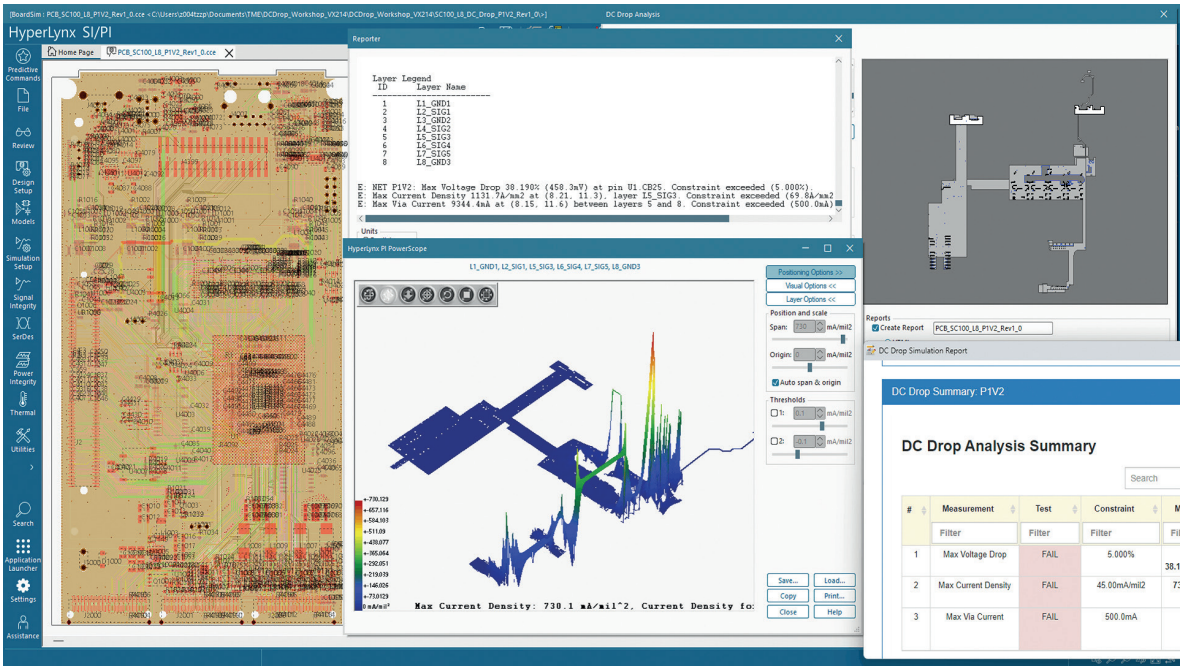
HyperLynx DC Drop

HyperLynx DC Drop ensures that designs operate reliably by analyzing multi-board power delivery systems for IR drop, current density and point to point resistance. This ensures adequate power is provided to each component and excessive current densities that could damage the board are avoided.

It analyzes current flow from the VRM to component power pins, ensuring that adequate voltage is supplied to components and excessive current densities are avoided. And it is fast enough to use interactively during PCB layout, so that problems can be detected and corrected early in the design process, when they are easier and faster to correct.

Both pre- and post-layout analysis are supported using a unique pre-layout editor that allows users to create and edit power planes, vias and signal topologies in a schematic-driven environment. This is ideal for performing basic PDN planning and experimenting with different scenarios. With a single analysis flow for both pre-layout design planning and post-layout verification, HyperLynx DC Drop makes it easy to compare pre- and post-layout analysis results, so that designers can compare their pre-layout expectations to actual post-layout behavior.

HyperLynx DC Drop eases the process of setting up analysis by bringing all power supply and component data together in one place. Users define power supply topologies, VRM characteristics and IC current draw, then HyperLynx does the rest. Multi-phase power supplies are supported, along with remote sense pins. Analysis results are presented in both interactive graphical and tabular report formats. The HyperLynx DC Drop report tells you exactly what you want to know most – what passed, what failed, and by how much.



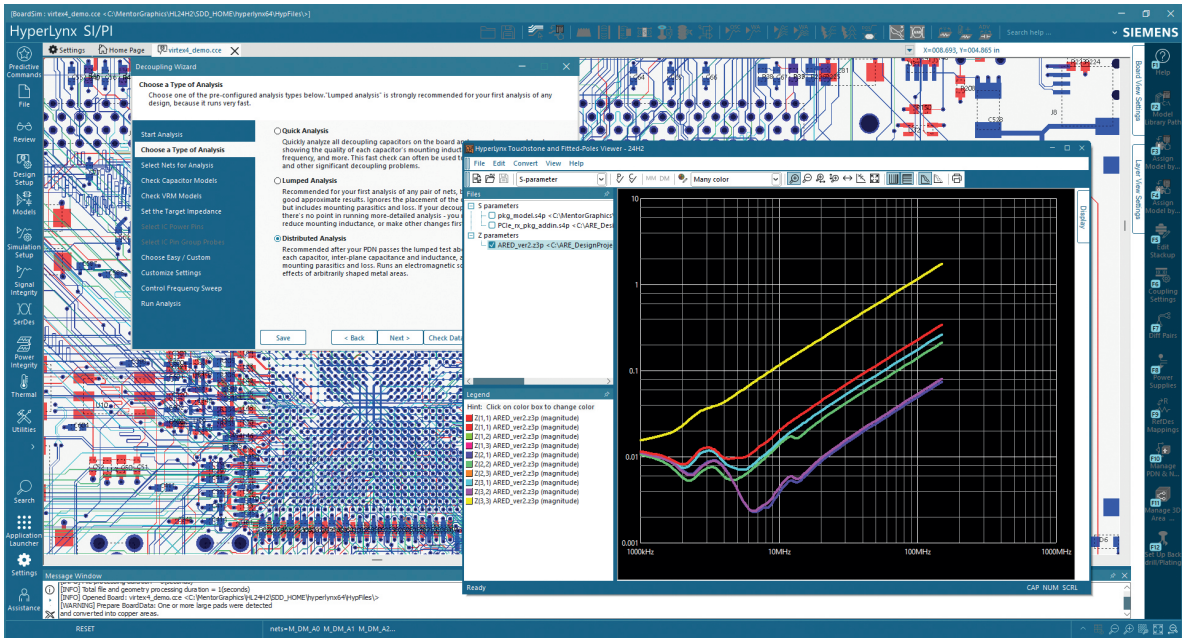
HyperLynx Decoupling Analysis

HyperLynx Decoupling Analysis models and analyzes PCB power delivery networks to ensure adequate voltage and current is provided at the necessary frequencies to support fast-switching characteristics of modern ICs. It reports PDN impedance at device power pins, along with pass/fail status.

HyperLynx advanced decoupling has industry leading analysis speed and database capacity, is easy to use with automated workflows, includes comprehensive reporting, and optionally includes the PDN Decoupling Optimizer.

HyperLynx advanced decoupling analysis evaluates the ability of a PDN to provide low-impedance paths for specific power supply pin pairs or pin group pairs. Advanced distributed PDN decoupling simulation accounts for the location of each decoupling capacitor, inter-plane capacitance and inductance, the board outline, and the mounting parasitics and loss for decoupling capacitors.

With automated post-layout extraction and analysis, HyperLynx Decoupling Analysis extracts and simulates a model of a design's entire PDN – displaying the PDN impedance as seen by each device of interest and reporting whether design requirements are met or not. Once the design has been set up and analyzed, changes can be made to improve performance and compare to earlier results.

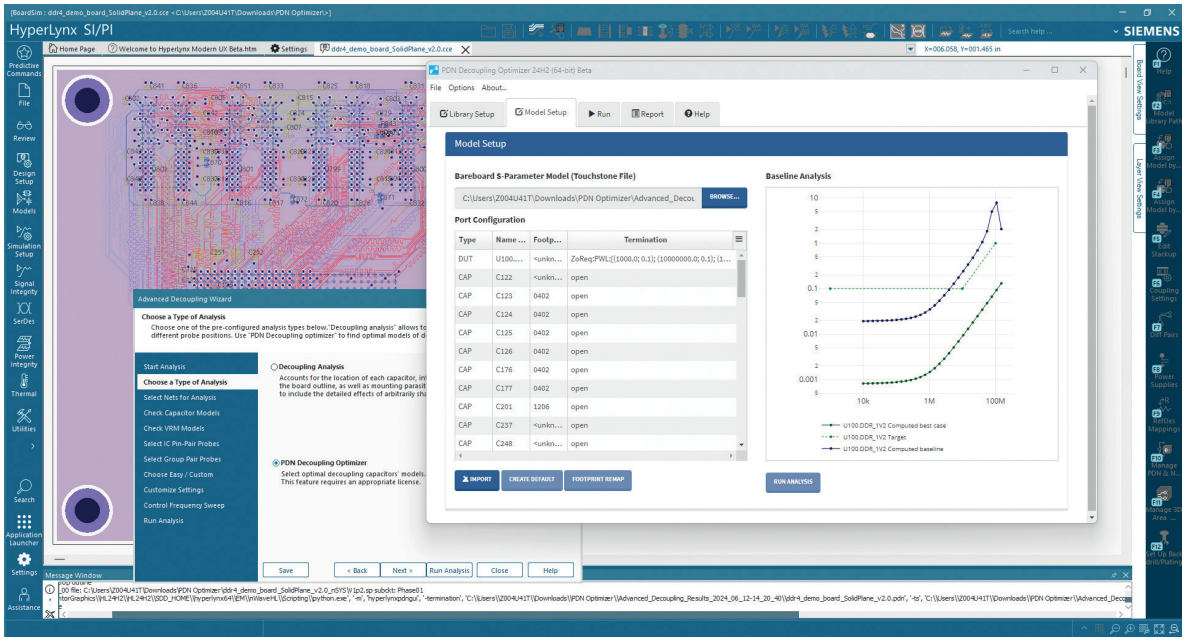


HyperLynx PDN Decoupling Optimizer

The HyperLynx PDN Decoupling Optimizer performs post-layout optimization of decoupling capacitor values and locations. The HyperLynx PDN Decoupling Optimizer efficiently optimizes a design for increased margin, reduced cost or part count, and increased physical routing space, using a combination of expert-based and genetic optimization algorithms.

HyperLynx advanced decoupling analysis evaluates the ability of a PDN to provide low-impedance paths for specific power supply pin pairs or pin group pairs. Advanced distributed PDN decoupling simulation accounts for the location of each decoupling capacitor, inter-plane capacitance and inductance, the board outline, and the mounting parasitics and loss for decoupling capacitors.

The HyperLynx PDN Decoupling Optimizer produces a hyperlinked, HTML report that lists all the different capacitor configurations analyzed, along with detailed performance, configuration and cost data for each. This allows designers to evaluate the tradeoffs between different potential solutions and pick the configuration that best meets their particular design goals.



Signal integrity analysis

Many PCB component interfaces are based on standards that define how signals are to be connected and what their electrical characteristics should be. If the signal traces conform to these specifications and the components meet or exceed the specifications, the interface should work.

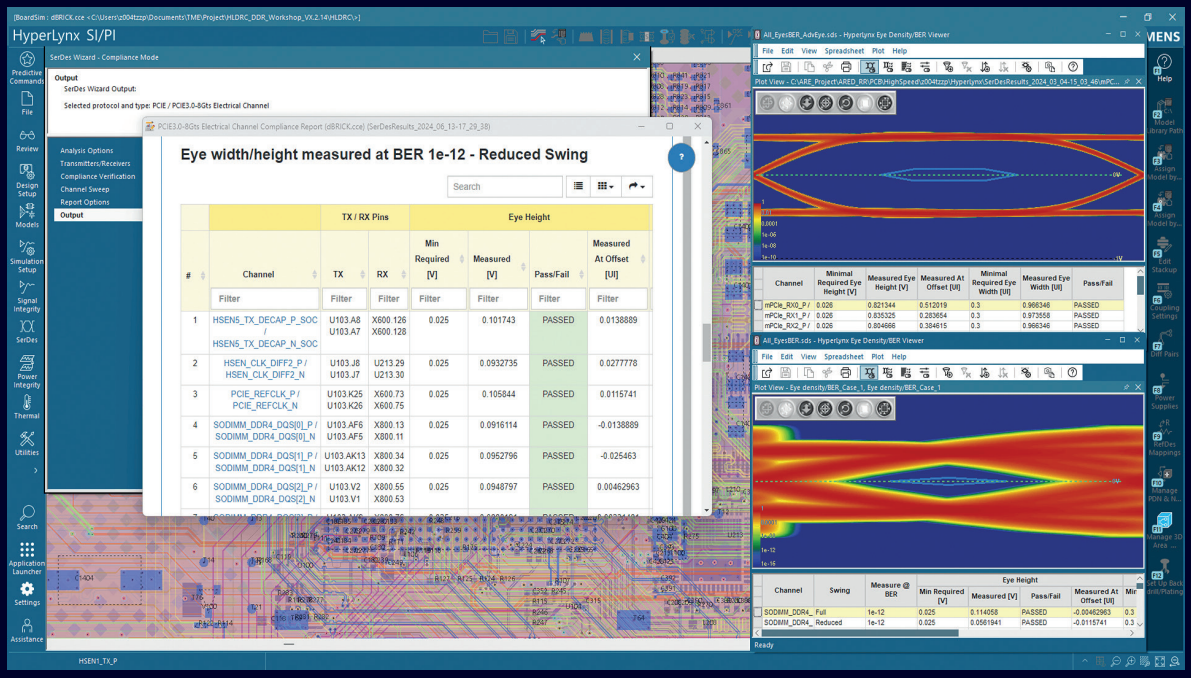
However, many interface standards specify electrical characteristics – such as impedance, loss, crosstalk, skew and eye openings – that require detailed modeling and simulation to predict. The need to consider signal integrity is pervasive in modern design. HyperLynx SI is an ideal solution for these issues.

HyperLynx SI is a complete signal integrity (SI) solution that simplifies and automates signal integrity analysis for high-speed digital pre-layout exploration and post-layout verification. HyperLynx SI makes sophisticated analysis more accessible to system designers, which in turn helps streamline the design process and reduce the workload of dedicated SI experts.

HyperLynx provides complete, interface-level analysis for DDR3-5 and LPDDR3-5 memories, simulating and analyzing signal quality and inter-group timing requirements. HyperLynx models controller-specific signal integrity and timing behaviors as part of the analysis.

The HyperLynx progressive verification methodology analyzes serial link interconnect for standards compliance, then uses IBIS-AMI models to perform device-specific analysis. Compliance analysis allows problems to be discovered earlier and easier than traditional analysis flows.

HyperLynx provides general-purpose signal integrity to predict signal quality and eye closure due to impedance mismatches and resulting inter-symbol interference, considering the effects of topology, drive impedance and slew rate, termination, signal spacing and crosstalk. Signals can be simulated and investigated individually, or entire groups of signals can be analyzed and reported in a batch analysis.



HyperLynx SI DDRx Design and Verification

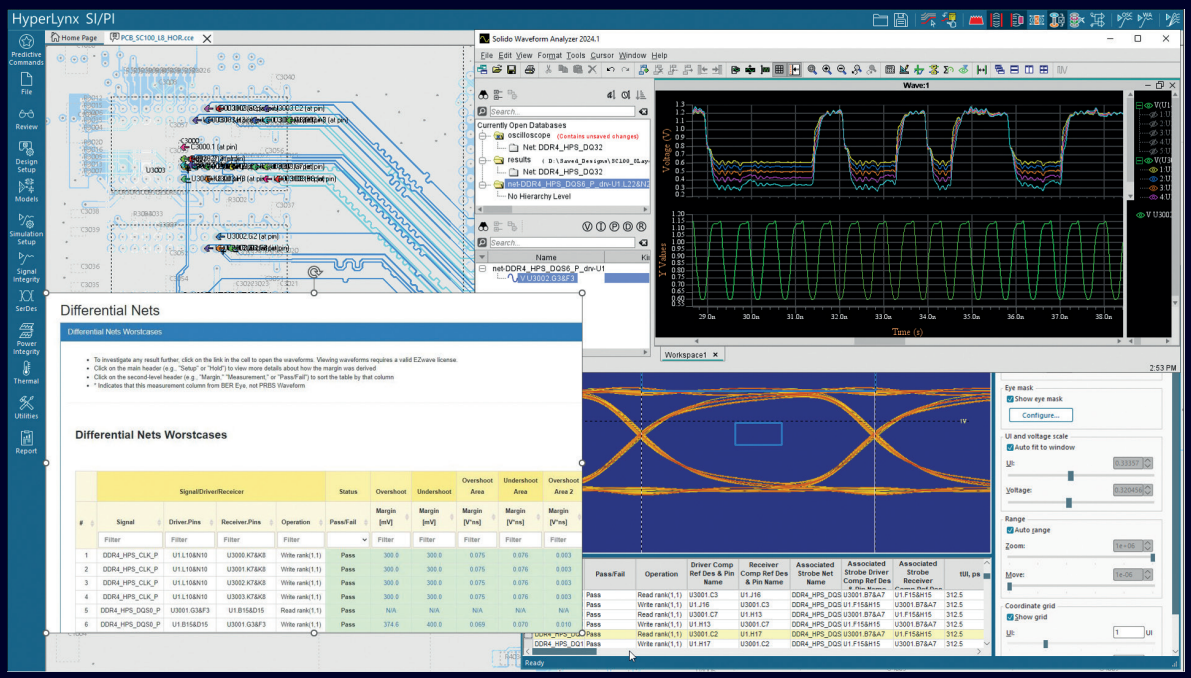
Ensuring that an interface will work requires ensuring that signal quality and timing requirements are met for all signals and inter-group relationships, including controller-specific behaviors. HyperLynx performs integrated signal integrity and timing analysis for double data rate (DDR) interfaces, verifying signal quality, skew and timing requirements. Automated layout extraction, 3D EM modeling and advanced simulation techniques support power-aware analysis and DDR5 applications.

HyperLynx pre-layout analysis lets designers explore the effects of routing order, termination, routing layers, via geometries and trace length/geometry/spacing on design performance. Importantly, it reports a design's voltage and timing margins as they will actually be measured in the system context.

HyperLynx fully automates full-interface DDR post-layout verification by combining automated layout topology extraction with advanced DDR protocol-aware simulation, comprehensive waveform post-processing and report generation.

Post-layout verification needs to perform the same analytical processes, and report results the same way as pre-layout exploration, so the two sets of results can be readily compared. HyperLynx SI DDRx unifies pre-layout and post-layout verification using the same automated analysis flow for each, so any issues that arise during layout can be quickly isolated and resolved.

HyperLynx DDR analysis produces a comprehensive report that lists the signals analyzed and shows what passed, what failed, and by how much. Results are filterable and sortable, allowing designers to quickly determine minimum/maximum values and isolate problem areas. The appropriate, protocol-specific eye mask can also be displayed to show the signal's voltage and timing margins.

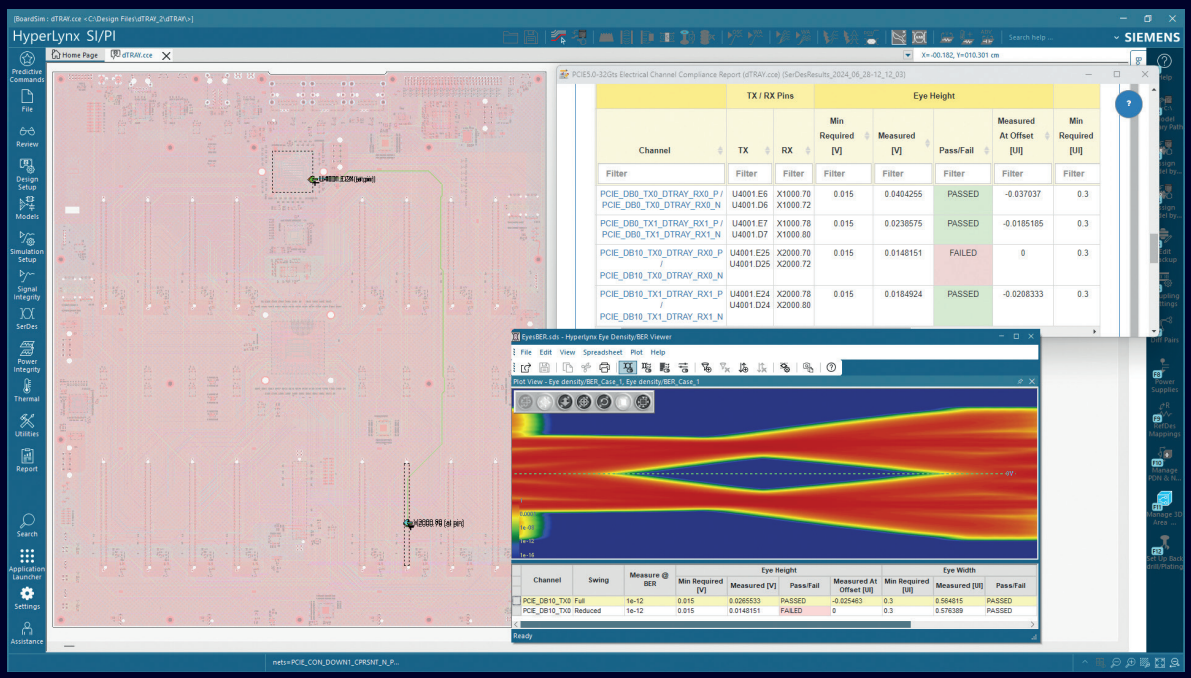


HyperLynx SI GHz

HyperLynx performs both standards-based interconnect compliance analysis and vendor model-based IBIS-AMI simulation for high-speed serial links. System-level, automated post-route analysis includes full topology extraction using integrated, 3D EM modeling with scalable performance.

Serial links must conform to requirements in associated standards specification documents. In each case, HyperLynx performs the standard-appropriate analysis flow and reports the metrics associated with each standard protocol. Each analysis type is specified via a built-in configuration file that automatically sets up channel speed, modulation, stimulus encoding, analysis flow and metric reporting for both compliance analysis and IBIS-AMI simulation. These configuration files can be copied and modified using a built-in editor, and new configurations can be added when available. HyperLynx also includes a set of generic setups that are useful for quick what-if analysis and prototyping support for new protocols.

HyperLynx automates the entire 3D EM modeling process – the designer specifies the signals of interest and criteria for identifying an aggressor signal – and HyperLynx does the rest. This process provides full channel modeling accuracy comparable to modeling the entire channel in a 3D solver, at a fraction of the compute and memory cost.



Electromagnetic simulation

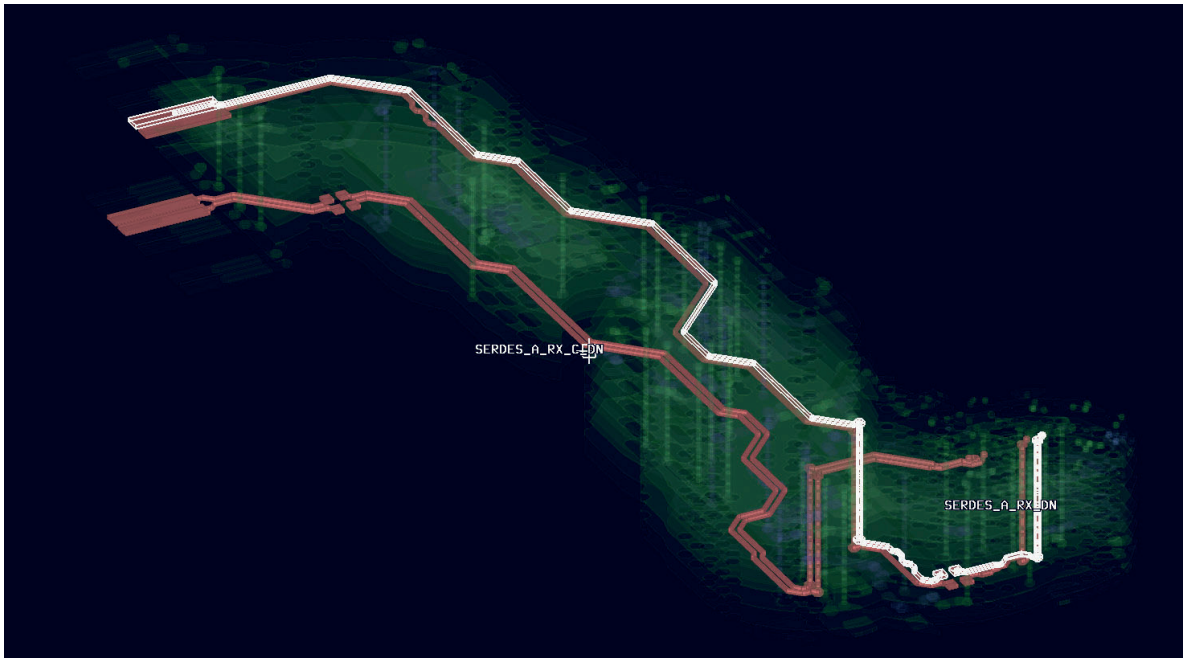
HyperLynx provides a complete family of electromagnetic (EM) simulation tools for PCB and IC packaging applications. These advanced solvers provide full-wave, hybrid and quasi-static simulation that can run standalone or as a tightly integrated part of signal and power Integrity analysis flows.

HyperLynx Advanced Solvers (HLAS) are tightly integrated with HyperLynx Signal Integrity and HyperLynx Power Integrity flows to provide accurate, automated interconnect modeling as part of a system-level analysis workflow. This allows DDR interface, high-speed serial channel and AC power integrity analyses to be performed with the highest levels of modeling accuracy. PCB models are extracted and solved automatically as part of these system-level workflows.

HyperLynx Full Wave Solver

The HyperLynx Full Wave Solver (FWS) is a boundary element solver used for simulating the very-high frequency behavior of 3D electromagnetic structures that have arbitrary geometries. It is one member of the integrated family of HyperLynx Advanced Solvers. In HyperLynx, the full-wave solver is typically used to model critical sections of high-speed serial channels, sections of high-density IC packages, or selected portions of DDR5 memory interfaces.

Full-wave solutions provide the most accurate simulations currently available. Full-wave approaches are used when the structure being analyzed is comparable (or larger) than the signal wavelength at the frequencies of interest. This is a general-purpose approach that doesn't make assumptions about the structure's geometry or its electromagnetic behavior.

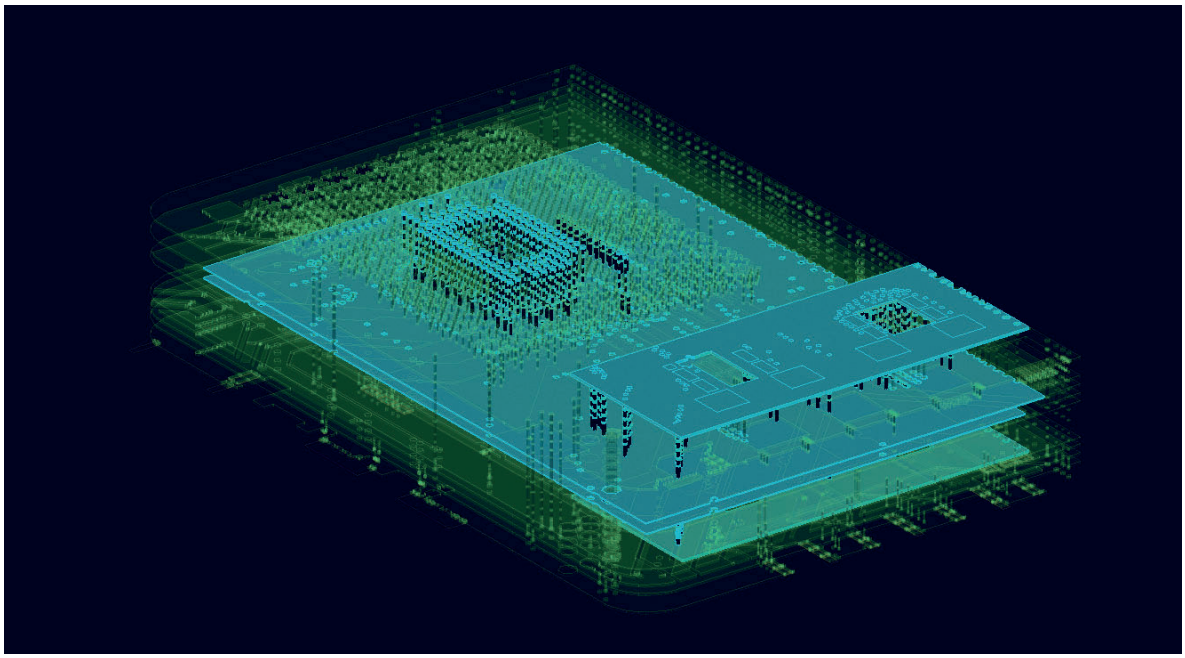


HyperLynx Hybrid Solver

The HyperLynx Hybrid Solver is a decomposition solver designed to create electro-magnetic models for layered electronic structures like PCBs and flexible cables. It is tightly integrated with HyperLynx signal and power integrity analysis to provide accurate, automated system analysis workflows.

Hybrid solvers are less compute and memory intensive than full-wave solving and can model larger structures as a result. A hybrid solver models the entire signal path and performs the decomposition in the solver.

The HyperLynx Hybrid solver is ideally suited for performing power-aware analysis of entire DDR interfaces, where capturing the effects of return path current sharing and Simultaneous Switching Noise (SSN) are important. It is also ideally suited for full-board AC power integrity, modeling decoupling capacitors and power delivery to IC pins. The Hybrid solver is especially well suited to power integrity because it models partial power planes and associated fringing effects.



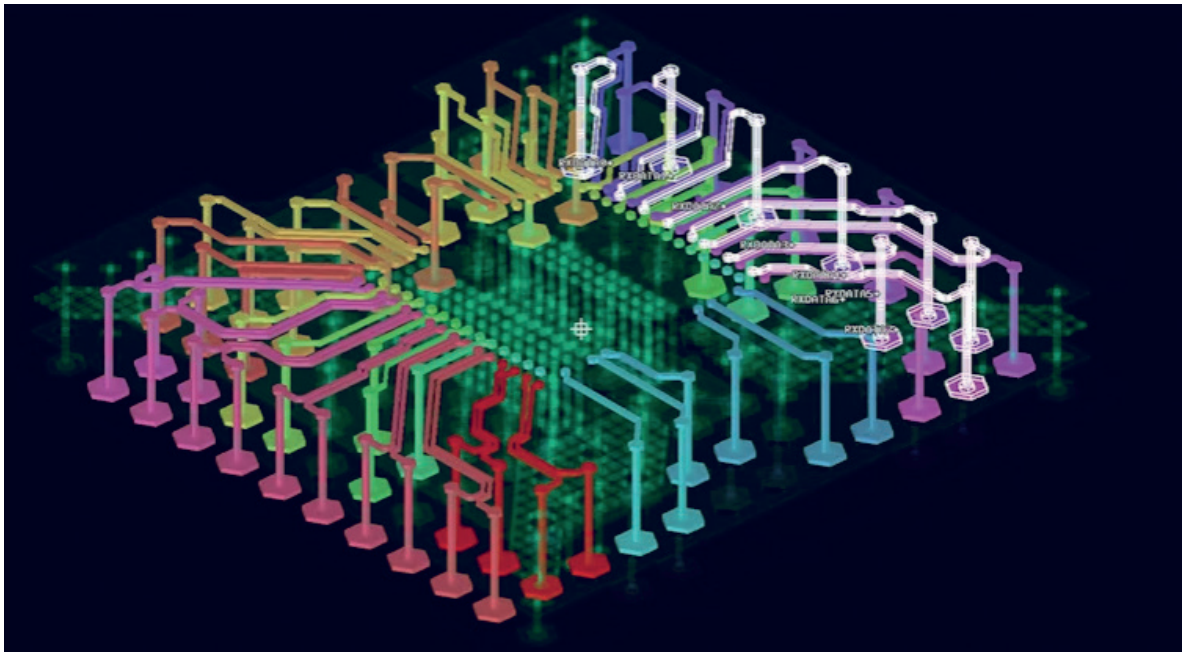
HyperLynx Quasi-Static Solver

The HyperLynx Fast 3D (Quasi-Static) solver extracts frequency-dependent resistance, inductance, capacitance and conductance values for electronic structures that are physically small compared to the wavelengths of interest, where time-varying elements of Maxwell's equations can be ignored. Because quasi-static methods solve the network at a single frequency point, they run faster and can handle larger structures than their full-wave counterparts.

The Fast 3D solver is integrated with Xpedition to support AMS simulation, using analysis to extract PCB parasitics from a Xpedition layout database and back-annotating them into the Xpedition Designer schematic. This workflow supports analog circuit and power module design and verification.

The Fast 3D solver can also be used standalone for package model extraction and simulation model creation. Package layouts can be directly imported from a variety of CAD formats, cropped, edited and solved, then exported using any of the simulation output formats that Fast3D supports.

The Fast 3D GUI provides an integrated environment for design import and editing, simulation setup and execution, followed by simulation results display, post-processing and export using multiple standard output formats. Multiple versions of a project can be created to test alternatives, then separately simulate projects and display results.



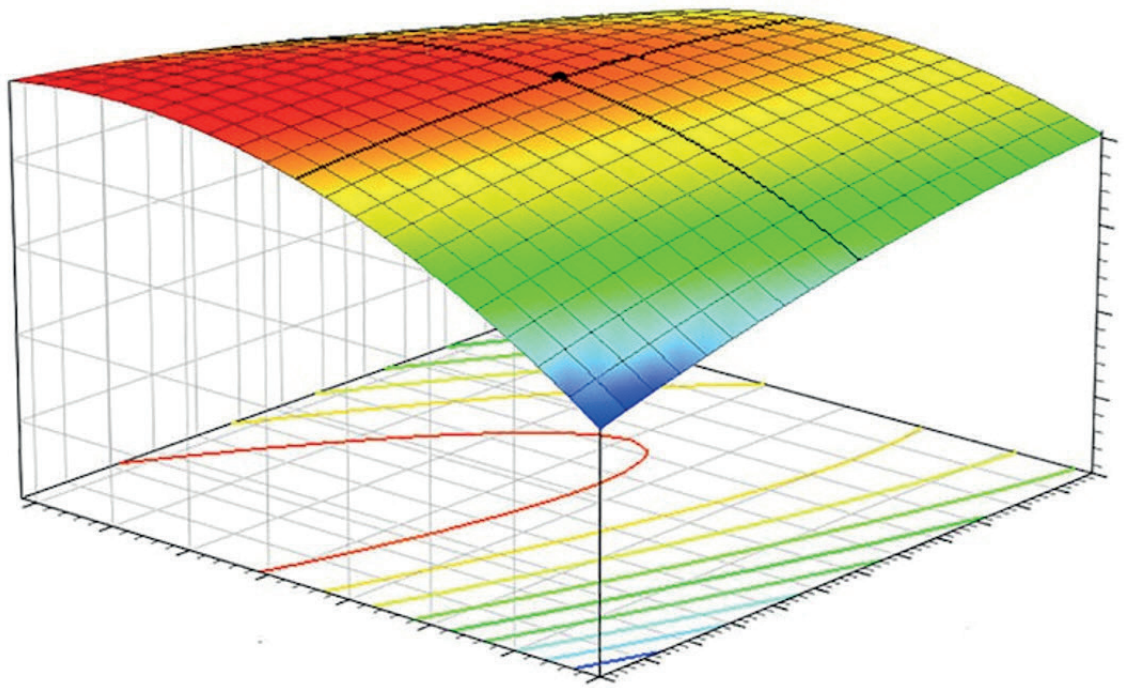
HyperLynx Design Space Exploration

HyperLynx Design Space Exploration (HL-DSE) provides advanced design optimization when the number of simulation cases to be investigated vastly exceeds what is practical. Efficiently exploring large design spaces with as few simulations as possible is a difficult task that requires a combination of advanced analysis techniques.

HL-DSE can find optimal solutions with a fraction of the computational resources required by traditional methods. A fitted mathematical, or *surrogate*, model is created that closely matches the designs input/output behavior within a parameter range. This surrogate model can then be in used in place of actual simulation experiments to predict the design's behavior over a large number of conditions, and therefore predict manufacturing yield.

The tool is integrated with both the HyperLynx Advanced Solvers 3D Explorer and HyperLynx Signal Integrity pre-layout serial link compliance flows. Output metrics already defined by the user are passed to HL-DSE, where the user adds pass/fail requirements and optimization goals.

HyperLynx Design Space Exploration offers a rich assortment of output plotting capabilities to provide insight into how a design behaves. These include 3D plots that can show things like how return loss is affected by via separation and antipad diameter.



Stackup design

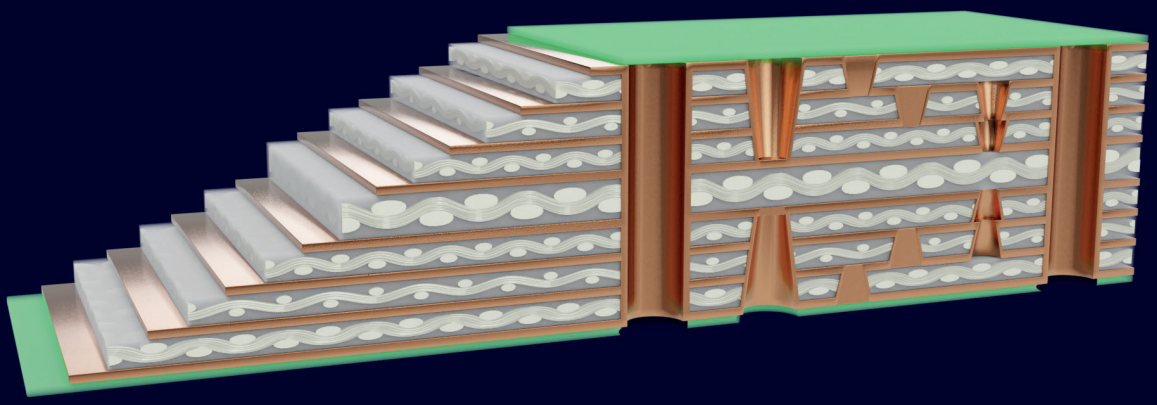
Z-planner Enterprise

Z-planner Enterprise is a stackup planning tool that includes a PCB stackup calculator focused on electrical impedance and signal integrity that helps you manage and optimize your PCB stackup design. It's library of PCB laminate material reduces material costs without sacrificing performance.

The tool provides complete control over the design and fabrication of a stackup, including an accurate field solver, a loss-planning environment, and a complete dielectric materials library. It optimizes the process of defining and documenting stackup requirements early in the design process, ensuring that pre-layout signal-integrity simulations are based on the most-accurate laminate data available using a consistent stackup design methodology. Stackup validation across multiple PCB fabricators is automated and final stackups can easily be exported for post-layout signal integrity signoff.

Z-planner Enterprise seamlessly interfaces with the most popular signal-integrity software and facilitates communication with all your fabrication houses. It also integrates seamlessly into the typical PCB design flow – from pre-layout signal integrity exploration to post-layout stackup verification across multiple PCB fabricators. Z-planner manages the entire process using an automation GUI that allows for automated validation and reporting.

Z-planner Enterprise comes equipped with an advanced stackup wizard that allows users to design and refine a multi-layer stackup quickly and comprehensively. It supports reusing proven stackups, saving time and improving the quality of those projects.



Summary

HyperLynx delivers a broad set of advanced capabilities covering design simulation, performance optimization, and verification analysis. Because it is interfaced to many PCB layout systems, HyperLynx allows you to quickly import and set up your PCB design for analysis. Whatever layout tool you use, high-speed post-layout verification is easier with HyperLynx.

With HyperLynx, there's no need for additional software, as it provides a complete set of analysis tools, pre-integrated, from a single vendor, along with proven workflows and examples. No switching formats, no isolated specialists, no bottlenecks.

HyperLynx works even better when it's an integrated part of a design flow that uses Siemens design capture and PCB layout tools within a full PCB design flow – from schematic capture through prototype fab-out and volume manufacturing.

HyperLynx includes proven automated analysis workflows that allow you to be productive "out of the box" and full system-level post-layout verification.

HyperLynx drives full-system post-layout verification with automated post-layout topology extraction, integrated 2D, 2.5D, and 3D electromagnetic modeling, and component and standards-based, protocol-specific simulation.

HyperLynx progressive verification finds issues faster and easier, analyzing a design in stages and locating issues early, without involving SI and PI experts.

HyperLynx scales from novice to expert, offering a broad variety of analysis capabilities and automated flows that make design analysis available to every user, regardless of individual skill level. This improves design quality and accelerates time to market.

Talk with your Siemens representative to learn how your electronics systems design team can leverage the analytic power of HyperLynx to tackle your most complex, modern designs.

Siemens Digital Industries Software helps organizations of all sizes digitally transform using software, hardware and services from the Siemens Xcelerator business platform. Siemens' software and the comprehensive digital twin enable companies to optimize their design, engineering and manufacturing processes to turn today's ideas into the sustainable products of the future. From chips to entire systems, from product to process, across all industries, Siemens Digital Industries Software – Accelerating transformation.

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